Vectorless Transient Power Grid Verification: A Case Study with IBM Benchmarks

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Abstract—Vectorless power grid verification is a powerful method that evaluates the worst-case voltage noises without detailed current waveforms by using optimization techniques. It is extremely challenging when considering transient current excitations, because transient currents are difficult to model and multiple time steps should be evaluated after the discretization of the system equation. In this work, we propose to perform vectorless verification with transient constraints and power constraints defined per clock period (or per hyper-period of multiple clocks if the grid supports multiple clock domains), so that the worst-case voltage noises of each node at any time step can be computed by transient simulation and solving optimization problems. More importantly, we apply the proposed transient verification approach to build a vectorless verification flow for IBM power grid transient analysis benchmarks, and evaluate the accuracy and runtime performance of the proposed approach with different hierarchical constraint setups. Experimental results show that the avg./max. errors of the proposed approach can be within 6%–9% of VDD, and the runtime to solve the optimization problems can be comparable to (or even larger than) the transient simulation time.

Index Terms—Power grid, vectorless verification, voltage drop, current constraint.

I. INTRODUCTION

As the technology scaling continues, power supply noises become increasingly important in modern chip designs, since the shrinking interconnect size leads to larger IR drops, and the high operating frequency results in substantial amount of Ldi/dt noises. Moreover, as supply voltages are lowered to reduce power consumption while subthreshold voltages are decreased for better performance, the gates have smaller noise margins, thus being more vulnerable to power supply noises than ever before. Hence, in order to ensure a robust chip design, it is indispensable to perform power grid verification in a modern design flow.

Traditionally, power grids are verified by simulation, and lots of works have been done to investigate efficient simulation techniques, e.g., [1]–[9]. However, power grid simulation often depends on the current waveforms extracted from the circuit implementation, thus can only be performed when the circuit implementation is available, while it is often preferred to verify the grid planning at early design stages for ease of modification. To satisfy this need, vectorless power grid verification techniques have been proposed [10]–[26]. These approaches use current/power constraints to model all possible current waveforms, and evaluate the worst-case voltage noises by solving optimization problems, which are usually large-scale linear programs.

Similar to power grid simulation, vectorless verification can also be performed under a DC model or a transient model. In DC model, only steady-state current constraints are considered for solving the worst-case voltage noises. This has been extensively studied and even featured by a white paper of Mentor Graphics [27]. The recent work [19] largely improves the scalability of vectorless verification under a DC model by using multigrid techniques. However, the vectorless verification in transient model is much less studied. Although hierarchical power constraints [23], [24] and transient current constraints [25], [26] have been recently proposed along with efficient solution techniques, which show the possibility of applying vectorless approaches for sign-off verification of power grids, we still have at least the following open questions?

1) How to properly model the current excitations and formulate the vectorless transient verification problem for efficient solution in a generic manner?
2) How to enable the verification of a node at any time step?
3) Are vectorless approaches accurate enough for practical use? (e.g., compared to power grid simulation techniques)

In this work, we target these open questions. Specifically, we employ transient constraints [26] and power constraints [23] for vectorless verification, and propose to define the time interval of transient and power constraints to be one operating clock cycle of the circuit, or the hyper-period of multiple clocks if the grid supports multiple clock domains. Moreover, we formulate the generic vectorless verification problem with transient and power constraints, so that each node can be verified at any time step by transient simulation and solving optimization problems. Most importantly, we have developed a vectorless verification flow for IBM power grid transient analysis benchmarks with hierarchical constraints by using the proposed approach. Extensive evaluation studies with different hierarchical constraint setups show that the avg./max. errors of the proposed approach can be within 6%–9% of VDD, and the runtime to solve the optimization problems can be comparable to (or even larger than) the transient simulation time.

The rest of this paper is organized as follows. Section II introduces the vectorless transient verification technique. Section III proposes the vectorless verification approach with transient and power constraints. Section IV presents the vectorless verification of IBM power grid transient analysis benchmarks. After experimental results are shown in Section V, we conclude the paper in Section VI.

II. PRELIMINARIES

A. Power Grid Model

We consider the generic RLC power grid model as illustrated in Fig. 1. It consists of both VDD and GND networks, where each network is basically an RLC circuit with attached current sources and VDD/GND pads. Each branch is either a resistor, a capacitor, or an inductor. The nodes in the VDD network are referred to as supply nodes, and the nodes in the GND network are referred to as ground nodes. Resistors and inductors are only located between two supply nodes or two ground nodes, while capacitors may also be located between a supply node and a ground node. The current sources attached to the grid model the behavior of the underlying circuitry, which draws current from the VDD network and injects current to the GND network. In this paper, we assume a single supply voltage, while this RLC power grid model and the proposed vectorless verification approach are also applicable for power grids with multiple supply voltages.

Let \( n \) be the total number of nodes that are not VDD/GND pads in the power grid, \( v_j(t) \) and \( I_j(t) \) be the nodal voltage and the current source at node \( j = 1, 2, 3, \ldots, n \), respectively. It is assumed that \( I_j(t) = 0 \) if node \( j \) does not have a current source attached, and the positive direction of current is from VDD to GND. Let \( \mathbf{V}(t) \) be the \( n \times 1 \) vector of current sources, and \( \mathbf{I}(t) \) be the \( n \times 1 \) vector representing the incoming current source of each node, i.e., its \( j \)th
element $\bar{I}_j(t)$ is defined as

\[
\bar{I}_j(t) = \begin{cases} 
-I_j(t), & \text{if node } j \text{ is a supply node}, \\
I_j(t), & \text{if node } j \text{ is a ground node}.
\end{cases}
\]

Let $\mathbf{v}(t)$ be the $n \times 1$ vector of voltage noises with its $j$th element $v_j(t)$, where $V_{dd}$ is the supply voltage. As derived in [25], the system equation of the power grid can be formulated as

\[
L\mathbf{v}(t) + G\mathbf{v}'(t) + C\mathbf{v}''(t) = \left(\bar{\mathbf{I}}(t)\right)',
\]

where $G$ is the $n \times n$ conductance matrix, $L$ is the $n \times n$ matrix similar to the conductance matrix but representing inductance values, and $C$ is the $n \times n$ matrix similar to the conductance matrix but representing capacitance values. According to [26], equation (2) can be discretized in time by using the trapezoidal rule [28] for vectorless verification.

**B. Current Constraints**

A variety of current constraints have been proposed to model the infinite many current waveforms in the power grid. Representative ones include local constraints, global constraints, transient constraints [25] [26], and power constraints [23] [24].

Since the maximum value of each current source is bounded, local constraints are introduced to define an upper bound for individual current source,

\[
0 \leq I(t) \leq I_L, \forall t,
\]

where $I_L \geq 0$ is an $n \times 1$ upper bound vector. In practice, it is never the case that all the gates or cells draw their peak currents simultaneously. Therefore, global constraints are introduced to define upper bounds for groups of current sources, i.e., the total current drawn by circuit blocks,

\[
U_GI(t) \leq I_L, \forall t, \text{ or } U_GI(k\Delta t) \leq I_L, \forall k,
\]

Let $m$ be the number of global constraints, then $U_G$ is an $m \times n$ 0/1 matrix indicating the assignments of current sources to groups, and $I_L \geq 0$ is an $m \times 1$ upper bound vector.

In order to capture the transient behavior of current sources, transient constraints are proposed in [25] to restrict the total amount of current (or more exactly "charge") that each current source can draw within a time interval, i.e., a number of continuous time steps. Let $N_{ts}$ be the number of time steps under consideration, then transient constraints can be formulated as

\[
\int_0^{N_{ts} \times \Delta t} \mathbf{I}(t) dt \leq I_T \times \Delta t, \text{ or } \sum_{k=1}^{N_{ts}} I(k\Delta t) \leq I_T,
\]

where $I_T \geq 0$ is an $n \times 1$ upper bound vector, and the integration operation is element-wise.

Power constraints are proposed in [23] to restrict the average power consumption of circuit blocks over a time interval. Consider $N_{ts}$ time steps, and assume that the current sources within circuit blocks are given by a 0/1 matrix $U_F$, then the corresponding power constraints can be represented as

\[
U_F \left( \int_0^{N_{ts} \times \Delta t} \mathbf{I}(t) dt \right) \leq \frac{N_{ts}^2}{V_{dd}} P_B \times \Delta t,
\]

or

\[
U_F \left( \sum_{k=1}^{N_{ts}} I(k\Delta t) \right) \leq I_F = \frac{N_{ts}}{V_{dd}} P_B.
\]

Here $P_B$ is an upper bound vector of block-level average power, and $I_F$ is the corresponding transient current limit.

Except for the aforementioned constraint types, some other constraints also have been proposed to better model the current excitations, including equality constraints [22], max delta constraints [29] and current slope constraints [30]. Typically, a combination of multiple constraint types is employed to model the current excitations for vectorless verification.

**C. Vectorless Verification Problem**

As studied in [20] and [22], the nodal voltage of an RC/RLC power grid can fluctuate in both directions, i.e., overshoot and voltage drop in the VDD network, ground bounce and undershot in the GND network. In many cases, overshoot and undershot cannot be neglected. They can be even comparable to voltage drop and ground bounce as shown in [26]. To verify the power grid conservatively, we need to evaluate the worst-case voltage noises in both directions.

Assume that there is no current excitation for all $t \leq 0$, so that $\mathbf{v}(t) = 0, \forall t \leq 0$. According to [20] and [23], for each node, the magnitude of the worst-case voltage noise is a non-decreasing function for all $t \geq 0$. Consider $k'$ time steps ($k' \geq 1$), then the vectorless verification is to solve the following optimization problem for each node $1 \leq j \leq n$,

\[
\text{Maximize/Minimize } v_j(k'\Delta t), \quad (5)
\]

subject to: the system equation (2) and $\mathbf{I} \in \mathcal{I}_F$, where $\mathcal{I}_F$ represents the feasible set of current excitations defined by current constraints. By maximizing the voltage noise, we get the worst-case overshoot or ground bounce. By minimizing the voltage noise, we obtain the worst-case voltage drop or undershot.

For efficient vectorless verification, it is proved in [26] that (5) can be decomposed into two sub-problems. For each node $1 \leq j \leq n$,

I: Compute $c_{j,k} = \mathbf{v}(k\Delta t)\mathbf{I}(k\Delta t) = \mathbf{e}_j, \mathbf{I}(k\Delta t) = 0, \forall 2 \leq k \leq k'$;

\[
\forall 1 \leq k \leq k';
\]

II: Maximize/Minimize

\[
v_j(k'\Delta t) = \sum_{k=1}^{k'} c_{j,k}^T \bar{\mathbf{I}}((k' + 1 - k)\Delta t), \quad \text{subject to: } \mathbf{I} \in \mathcal{I}_F. \quad (7)
\]

Here $\bar{\mathbf{I}}(t)$ is the vector of incoming current sources at each node defined in (1); $c_{j,k}$ is an $n \times 1$ vector, which represents the voltage responses at time $k\Delta t$ if we apply an impulse current excitation on node $j$ at time $\Delta t$. Clearly, the first sub-problem is a power grid transient analysis problem with an impulse current on the node to be verified, thus can be efficiently solved by existing transient analysis algorithms. Then the major challenge is to solve the optimization problems in the second step efficiently.

**D. Related Works**

To reduce the complexity of solving the optimization problems, [23] uses hierarchical power constraints for verifying the grid, so that the optimization problems (7) can be efficiently solved by a sorting-deletion algorithm; [26] employs transient constraints and hierarchical
global constraints, and proposes a variable reduction scheme for solving the optimization problems with a user-specified error tolerance. Besides, [24] proposes to use the model order reduction technique for efficient transient simulation in order to calculate \( e_{j,k} \).

These works consider transient or power constraints over a time interval, e.g., 100 time steps with a step size of 10ps, and solve the worst-case voltage noise within it. The experimental evaluations are against the verification without transient or power constraints to demonstrate the effectiveness of the proposed approaches. However, the following questions are still open:

1. **How to determine the proper time interval for transient and power constraints?**
   I.e., how to choose a proper \( N_{ts} \) for (3) and (4)?

2. **For a given time interval of transient or power constraints, how to compute worst-case voltage noises at later time points?**
   I.e., given the transient or power constraints for \( N_{ts} \) time steps, how to calculate \( v_j(k'/t), \forall k' > N_{ts} \)?

3. **Compared with power grid transient simulation with extracted current waveforms from the circuit, how accurate are these vectorless verification approaches?**

These are fundamental questions regarding to the application of vectorless verification techniques. In this work, we propose a novel transient verification mechanism to address the first two questions. Moreover, in order to give some insights on the third question, we evaluate the proposed vectorless verification approach by using the IBM power grid benchmarks.

**III. VECTORLESS TRANSIENT POWER GRID VERIFICATION**

**A. Time Interval for Transient and Power Constraints**

We propose that the time interval for transient and power constraints should be one operating clock cycle of the circuit, because a clock cycle is the basic time period for circuit switching. At early design stages, we may get some reasonable estimations of local, global, transient and power constraints according to the current/power intent of the chip. When the circuit implementation is ready, switching activity analysis [31] can be performed to derive the maximum amount of switching instants for each gate/cell within a clock cycle, then these switching instants are translated into current waveforms, which are finally discretized to get the upper bounds of transient constraints. Similarly, power analysis can be performed to derive proper power constraints. As local and global constraints represent the peak values of current sources and the peak power of circuit blocks, they can also be extracted by switching activity analysis and power analysis. With these constraints extracted from the circuit, we can apply vectorless approaches for sign-off verification of power grids, e.g., to verify some nodes in the risky region.

As it is common that a chip has multiple clock domains, so that different circuit blocks can work at different frequencies, we propose that the time interval for power constraints over multiple clock domains should be the hyper-period, i.e., the least common multiple among all periods of the corresponding clocks. In this way, a grid with multiple clock domains can also be properly verified.

**B. Proposed Problem Formulation**

With a proper time interval for transient and power constraints, a group of transient and power constraints can be introduced for each non-overlapped time interval as shown in Fig. 2. Based on such constraint structure, we can effectively solve the worst-case voltage noises at any time point.

Specifically, by considering a combination of local, global, transient, and power constraints, (7) can be re-written as

Maximize/Minimize \( v_j(k' \Delta t) = \sum_{k=1}^{k'} e_{j,k} \bar{I}((k' + 1 - k) \Delta t) \)  \( \text{(8)} \)

subject to: \( 0 \leq I(k\Delta t) \leq I_L, U_G I(k\Delta t) \leq I_G, \forall k; \)

\[
\sum_{k=p\times N_{ts}+1}^{(p+1)N_{ts}} I(k\Delta t) \leq I_T, \forall p \geq 0;
\]

\[
U_P \left( \sum_{k=p\times N_{ts}+1}^{(p+1)N_{ts}} I(k\Delta t) \right) \leq I_P, \forall p \geq 0.
\]

Obviously, (8) is a linear programming (LP) problem since the objective function and all the constraints are linear. It is to be noted that each time step has a group of local and global constraints, and each time interval \([ (p \times N_{ts} + 1) \Delta t, (p + 1) \times N_{ts} \Delta t ] \) has a group of transient and power constraints. There is no constraint to relate the current variables of different time intervals. Hence, (8) can be further decomposed and solved for each time interval.

However, despite further problem decomposition, the number of decision variables for the LP problem over a single time interval is still up to \( N_{ts} \) times the number of current sources. Consider that \( N_{ts} \) is often no less than 100 in practice, and we may have millions of current sources in large-scale power grids, solving such large-scale LP problems by a standard LP solver to verify a single node can be prohibitive. More research needs to be done in order to solve the LP problems efficiently. In this work, we propose this generic methodology for vectorless transient verification, and then evaluate the proposed approach with IBM power grid transient analysis benchmarks.

**IV. TRANSIENT VERIFICATION OF IBM POWER GRIDS**

**A. Vectorless Verification Flow**

As the current sources in these IBM power grids are all pulses with non-zero DC bias, which represent the static current drawn by the circuit, we first perform DC analysis to calculate the DC voltage of each node \( j \), denoted as \( u_j \), and then remove the DC bias from each current source for extraction of current constraints, so that we have a zero initialization condition for vectorless verification, and the problem formulations discussed in previous sections can be directly applied. Fig. 3 presents the overall vectorless verification flow. For each node \( j \) to be solved, we perform transient simulation with the corresponding impulse current excitation \( I(\Delta t) = e_j \) to calculate the constant coefficients \( c_{j,k} \), and then solve the LP problems (8) subject to proper current constraints to obtain the worst-case voltage noises within the verification time period. Let \( v_{j,min} \) and \( v_{j,max} \) be the computed minimum and maximum voltage noise at node \( j \), respectively, then the actual voltage level at node \( j \) is bounded by \( u_j + v_{j,min} \leq v_j \leq u_j + v_{j,max} \), where \( u_j + v_{j,min} \) and \( u_j + v_{j,max} \) are reported as the lower and upper bounds of voltage levels at node \( j \), respectively.
We first experiment with different constrained time interval sizes for transient and power constraints. Fig. 7 presents the corresponding underestimation of voltage noises for ibmpg1 with “local+tran+ierPower”. Note that ibmpg1 has current sources with periods of 2ns and 3ns. As expected, setting the time interval size to be the hyper-period of 6ns achieves the best accuracy, and further increasing the time interval size does not yield a better solution. This
confirms our proposal for setting the constrained time interval sizes in Sec- 
section III-A. Similar phenomena is also observed for overestimation and 
the experiments with “local+global+HierPower”, as well as other 
power grids except ibmpg4t. Because ibmpg2t, ibmpg3t, ibmpg5t and 
ibmpg6t also have current sources with periods of 2ns and 3ns, while 
ibmpg4t just has current pulses with a period of 3ns. Hence, we set 
the constrained time interval of ibmpg4t to be 3ns, while setting the 
constrained time interval of other power grids to be 6ns in all the 
other tests.

Another set of experiments are performed to evaluate the effect 
of the levels of constraint hierarchies on solution accuracy. As 
shown in Fig. 8, the underestimation of voltage noises decreases 
when we increase the levels of global constraints. The tests with 
“local+global+HierPower” show similar phenomena since the global 
constraints are at finer granularity when we more levels of constraints 
are extracted. However, in the tests with “local+tran+HierPower”, 
results show that the solution accuracy is independent of the levels 
of power constraints.

In fact, the power constraints in Fig. 6, and the high-level power 
constraints in Fig. 5 have no effect on the verification results. 
That is attributable to the fact that upper bound vectors of power 
constraints are directly computed by using the current waveforms 
(with the constrained time interval being the unique current period 
or the hyper-period of current sources). A current vector satisfying 
the transient constraints or the lower-level power constraints would 
naturally satisfy the power constraints above. Hence, in our setting, 
“local+tran+HierPower” is equivalent to local constraints + transient 
constraints; while “local+global+HierPower” is equivalent to local 
constraints + global constraints + lower level power constraints. 
Fortunately, these simplified constraint setups enable us to probe more 
insights about the effects of constraints on vectorless verification, and 
the verification runtime would still indicates the cost of vectorless 
verification with “local+tran+HierPower” and “local+global+HierPower” 
due to the underlying implementation.

The performance tests are performed with four levels of constraint 
hierarchies, i.e., each network has up to 15 hierarchical global/power 
constraints. As shown in Fig. 9, the computed bounds of voltage 
levels enclose the actual simulation waveform, which confirms the 
effectiveness of the proposed approach. Table I presents the accuracy 
results of vectorless verification with different constraint 
setups; “local+HierGlobal” often has the largest underestimation and 
overestimation; “local+Global+HierPower” often has the best accuracy

except a few cases, where “local+tran+HierPower” shows the smallest 
average underestimation or overestimation for ibmpg3t, ibmpg4t, and 
ibmpg6t. Clearly, the computed bounds of voltage levels provided by 
“local+HierGlobal” are way too off consider that the VDD voltage 
is 1.8V in these power grids. With these three constraint setups, 
the best avg./max. underestimation is within 94mV/150mV, while the 
best the avg./max. overestimation is within 1085mV/157mV. Such 
error magnitudes are within 6%/9% of VDD, which are still large 
consider that we may just accept minor voltage drops in the grid, 
e.g., within 5%. Hence, it is still important to perform vectorless 
verification with a combination of local, global, transient, and power 
constraints to further reduce the error.

Table II lists the vectorless verification runtime. Most of the 
running time are due to transient simulation to calculate the constant 
coefficients c_{j,k} and solving the LP problems (8) to obtain the 
worst-case voltage noises. Except these two parts, the other runtime 
components include “loading the power grid”, “DC analysis”, “ex- 
tracting the current constraints”, and “LU decompostion for transient 
simulation”, etc. Those are excluded from the table for simplicity of 
illustration. With “local+HierGlobal”, we can solve a decomposed LP 
problem at each time step, so the corresponding runtime for solving 
the LP problems are smaller than that of “local+global+HierPower” 
and “local+tran+HierPower”. Note that even with the sorting-deletion 
algorithm, the runtime for solving the LP problems for vectorless 
verification can be comparable to (or larger than) the corresponding 
transient simulation time, e.g., ibmpg6t. This motivate us to study 
more efficient vectorless verification algorithms for practical use.

VI. Conclusion

In this work, we have presented a vectorless verification tech- 
nique with transient constraints and power constraints defined per 
block clock (or per hyper-period of multiple clocks if the grid 
supports multiple clock domains). The proposed approach has been 
employed to build the vectorless verification flow for IBM power grid 
transient analysis benchmarks. Experimental results have confirmed 
the effectiveness of the proposed approach, and it is shown that 
vectorless verification with transient or power constraints still have 
poor accuracy and large running time. Future work would be to 
further improve the accuracy and runtime efficiency of vectorless 
verification approaches.

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TABLE I

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